Lenkurt®

26C DATA SET

duobinary-datatel™

The 26C Data Set is an economical and highly accurate modulator-demodulator for transmitting serialized digital data at speeds of 1200 or 2400 bits per second (bps) over a standard 3-kc voice channel. The voice channel can be derived on cable, open-wire, carrier telephone, or microwave radio transmission facilities. Transmission at 2400 bps is achieved with Lenkurt's unique Duobinary coding technique applied to a synchronous FSK carrier wave. Transmission at 1200 bps is accomplished by synchronous binary FSK modulation. In both the binary mode and duobinary mode of operation, the transmitted signal is synchronous FM with a nominal line frequency of 1200 to 2400 cps.

Duobinary coding doubles the data-handling capability of standard 3-kc voice circuits and also enables automatic error detection plus a very low error rate to be achieved at speeds of 2400 bps.

Full-Duplex Data Set
Installed in Portable Cabinet

SIMPLE INSTALLATION — All connections to external equipment (power, data, and transmission lines) are terminated at quick-disconnect connectors. This permits installation or changeout of a complete Data Set in a matter of minutes.

AUTOMATIC ERROR DETECTION — With the Duobinary technique, binary data is encoded in such a way that the transmitted signal follows a predetermined pattern. At the receiver automatic error detection is achieved by simply monitoring this pattern—redundant bits for parity checking *do not* have to be added to the data stream.

SPEED PLUS BANDWIDTH ECONOMY — The data handling capability of a standard 3-kc voice channel is *doubled* with the Duobinary technique. Specifically, the 26C can transmit data at a 2400 bps rate in the same bandwidth required for transmitting data at 1200 bps with standard binary systems.

SMALL SIZE — A full-duplex data set weighs less than 20 pounds and requires only 3½ inches of height in a standard 19-inch wide equipment rack. The 26C can also be supplied in a small cabinet suitable for placing on a table, desk, or shelf near the computer or data terminal equipment.

SYSTEM COMPATIBILITY — The 26C accepts and provides data signals that meet EIA Standard RS-232-A and MIL-STD-188B interface requirements. Options are provided to meet other customer requirements.

EASY MAINTENANCE — Modular construction, solid-state components, integrated circuitry, double-sided printed circuit boards, and the Duobinary coding technique combine to provide a modem that is highly reliable, small in size, and easy to maintain. Indicators are visible with the front cover closed. All controls and test points are clearly marked and easily reached when the cover is open.

ACCURATE — Because of low intersymbol interference — a product of the Duobinary technique and synchronous FSK modulation — the 26C has an extremely low error rate. Operating at 2400 bits per second over a very noisy channel (13 db signal-to-noise ratio) the average error rate is only one bit in one-hundred thousand (1 bit in 10^5).

FLEXIBLE — The 26C can be equipped for full-duplex, simplex-transmit, or simplex-receive operation. If requirements change after installation, a simplex configuration can be easily expanded to duplex by merely adding plug-in units.

TYPICAL APPLICATIONS

GENERAL — The 26C Data Set can be used in a wide variety of applications where transmission of serialized digital data at speeds of 1200 or 2400 bits per second is required. Typically, the 26C is used for one-way or two-way data transfer between digital computers. Other practical applications include telemetering, digitized voice or facsimile data transmission, and air-to-ground data communications over VHF or UHF radio links.

Because of its economical use of the voice frequency bandwidth, the 26C can transmit data accurately over FCC Tariff 237 schedule 4A telephone network facilities or any other voice frequency transmission facility that meets the line requirements specified in the technical summary.

INPUT/OUT CONSIDERATIONS — The 26C accepts serial binary data in the non-return to zero (NRZ) format. The input and output voltage levels and impedances meet the standard data interface (low-level) requirements specified in MIL-STD-188B. Strapping options are provided to meet the input/out data interface requirements recommended in EIA Standard RS-232-A.

The 26C can be easily adapted to accommodate data signals which are not in accordance with EIA recommendations or military requirements. If necessary, custom-designed interface converters can be provided to match input and output requirements specified by the customer.

TIMING SOURCES — A clock signal is required in the transmit branch of the 26C Data Set for

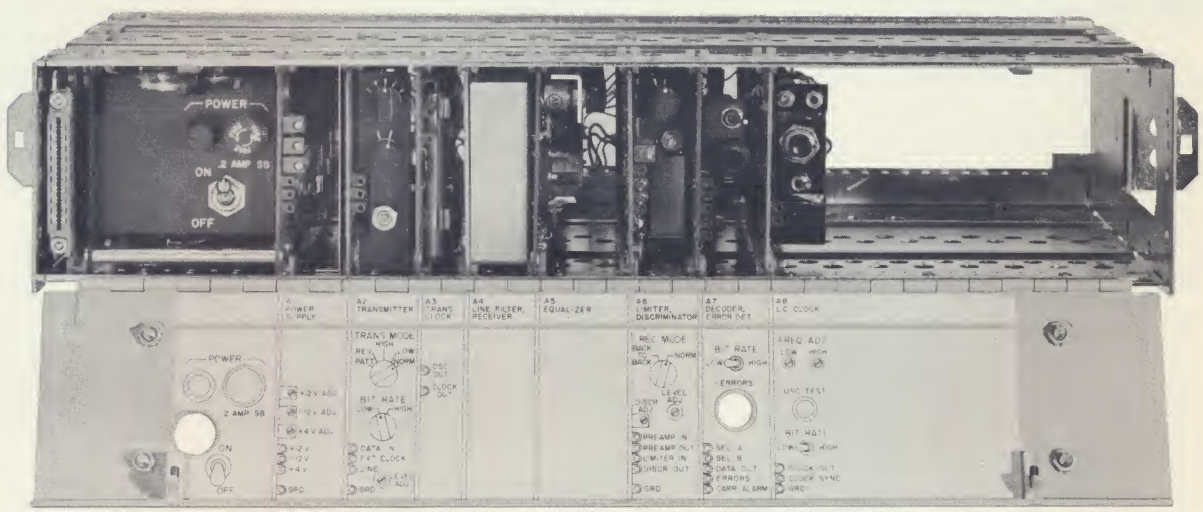

Figure 1. Fully equipped Data Set with front cover lowered to show plug-in units. Note the Extender Unit mounted at the left of the Power Supply Unit.

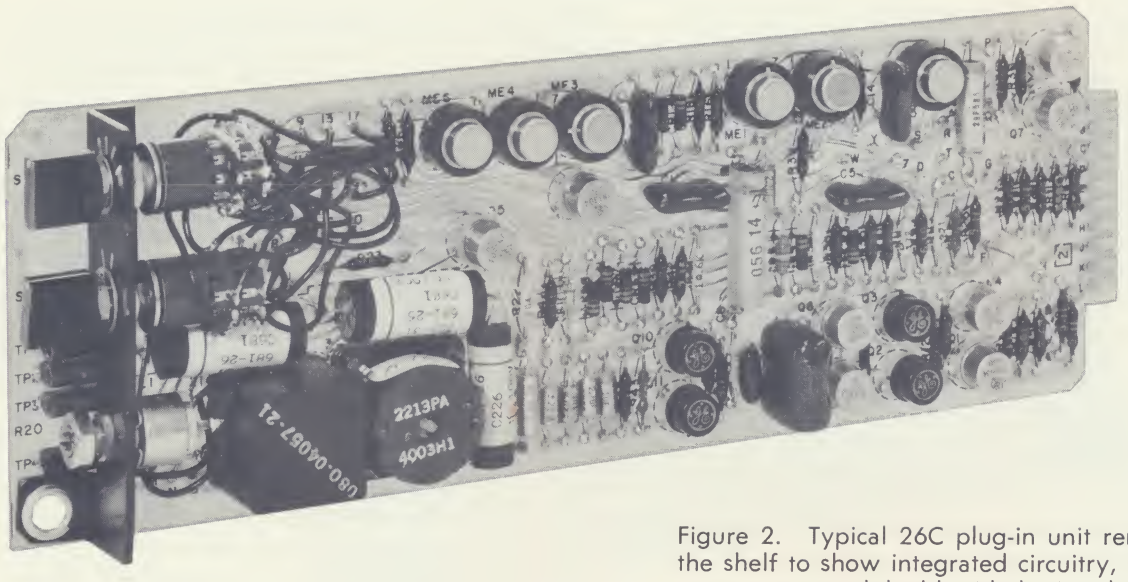

Figure 2. Typical 26C plug-in unit removed from the shelf to show integrated circuitry, miniaturized components, and double-sided printed circuit board. Note the switch, adjustment control, and test points located on the face of the unit for easy access during operation.

encoding 2400 bps data inputs and for FSK modulation of the binary and duobinary signals to produce a synchronous FM line signal. In the receive branch, a clock is used to retime the data and is required for operation of the Duobinary error detector.

Plug-in transmit and receive clock modules are available as an integral part of the 26C Data Set. The transmitter clock has a frequency stability of 0.01%, and the receiver clock is synchronized to the transmit clock frequency by received data transitions. In the absence of data transitions the receiver clock remains locked to the last received frequency for at least 2400 bit periods. This frequency stability equals or exceeds the requirements of most data transmission systems. If required, an optional clock shelf and power supply can be furnished to provide transmit and receive clock signals with a frequency stability of *5 parts in 100 million per hour.* In the absence of received data transitions, this clock will remain locked to the transmitted frequency for at least 30 minutes.

An external clock may be used in the transmit branch provided it has a frequency stability equal to or greater than the clock used in the receive branch. (See Technical Summary)

SYSTEM DESCRIPTION

MODULAR PLUG-IN UNITS—The 26C Data Set comprises plug-in units that are modular by function. Therefore, the Data Set can be equipped to meet the exact functional requirements of each application at a minimum cost. For example, the 26C can be equipped for full-duplex, simplex-transmit, or simplex-receive operation with or without clocks depending on customer requirements. For ease of expansion and flexibility, each Data Set is fully wired for all plug-in units including the optional transmit clock, receive clock and adjustable line equalizer. (See Table C.) Thus, should customer requirements change after a system has been installed partially equipped (for example, simplex-transmit), the capabilities may be easily expanded by merely adding plug-in units.

INSTALLATION FEATURES — A full-duplex Data Set, including power supply, adjustable equalizer, transmit clock, and receive clock, weighs less than 20 pounds and requires just 3½ inches height —two rack mounting spaces—and 10 inches depth in a standard 19-inch wide equipment rack. Also a complete self-contained full-duplex Data Set can be supplied in a small portable cabinet suitable for

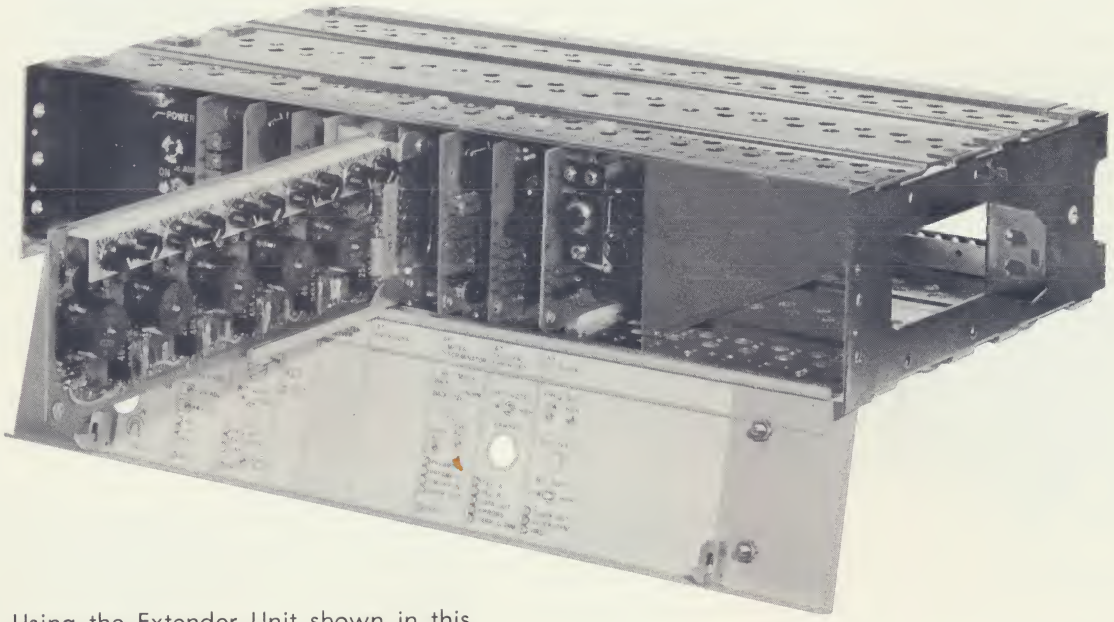

Figure 3. Using the Extender Unit shown in this figure, plug-in units may be withdrawn from the shelf for alignment, testing, or check-out while the equipment is in operation.

placing on a table, desk, or shelf near the computer or data terminal equipment.

All connections to external equipment including power, data terminal equipment, and line facilities are made to quick-disconnect connectors at the rear of the modem. These connectors permit installation or changeout of a complete Data Set in a matter of minutes.

MAINTENANCE AND OPERATION FEATURES — High reliability and minimum maintenance are assured by the use of solid-state components and printed circuits. The 26C is miniaturized and uses micrologic modules where ever possible to reduce the total number of components. All commonly used test points, controls, and indicators are accessible from the front of the equipment, and are clearly identified by a printed card attached to the inside of the front cover.

A built-in test pattern generator provides random binary data for testing and alignment, and a Duobinary error detector monitors transmission quality. An indicator lamp on the error detector enables operators to visually monitor errors — no external equipment is required.

A loop-back switch is provided on the 26C limiter-discriminator unit to connect the output of the transmit branch to the input of the receive branch. (The adjustable equalizer unit is bypassed since it is used to correct for delay and amplitude distortion introduced by the transmission line.) The loop-back switch, in conjunction with the test pattern generator and error detector, can be used to quickly align or test a 26C Data Set independent of the distant terminal. Also, in event of transmission trouble, it provides a means of quickly localizing the trouble to its source: the transmission facility, the data terminal equipment, or the applicable data set.

An extendor unit is available to extend 26C plug-in units from the shelf for testing or maintenance while they are in operation. (See figure 3.)

SYSTEM OPERATION

MODULATION PLAN — The 26C utilizes synchronous FSK modulation for transmission of 1200

and 2400 bits per second serial data over wire lines. At the 1200 bps speed ordinary binary transmission is employed. For 2400 bps operation, the Lenkurt-invented Duobinary technique, a unique encoding process, provides a two-to-one bandwidth compression of 2400 bits per second data to supply a transmitted frequency spectrum equal to that of the binary spectrum.

Line frequencies derived from the transmit clock (no additional transmit oscillator is required) at the 1200 bps rate are 2400 cps for the MARK level, and 1200 cps for the SPACE level. At the 2400 bps rate, the line frequencies are 2400 cps or 1200 cps for MARK, and 1800 cps for SPACE.

TRANSMIT BRANCH — The serial binary data input to the modem is converted into an FSK wave using binary transmission for 1200 bps, and Duobinary encoding for 2400 bps. In the 2400-bps Duobinary mode of operation, the data is encoded using either an internal or external clock.

After FSK modulation, the encoded signals (both binary and Duobinary) are amplified, filtered, and then coupled to the voice channel transmission line.

Because the line frequencies are derived from the transmit clock and because the data transitions must be synchronous with the transmit clock frequency, either the 26C transmit clock module or an external clock signal must be supplied. If an external clock is used it must be synchronized with the data input.

RECEIVE BRANCH—In the receive direction, the input FM signals are amplified and filtered and then applied to the adjustable line equalizer. The equalizer corrects for both delay and amplitude distortion introduced by the transmission line. The delay distortion adjustment range is 2.5 milliseconds for frequencies between 900 and 2700 cps. After the equalizer, the signals are amplitude limited and applied to a discriminator. The discriminator converts the FM signal into an analog voltage which is then filtered and applied to level selectors. Two level selectors are used; only one is needed for the binary rate, but both are used for detection of a duobinary signal. The signals are then fed into the decoder where they are converted back into their original serial-by-bit binary data form.

When operating in the Duobinary mode, the outputs of the two level selectors are also fed into the error detector along with the signal from the receiver clock. Th error detector monitors the Duobinary coding pattern for violations caused by disturbances in the transmission path. Whenever a pattern violation occurs, an error pulse is generated which light the ERRORS lamp on the front of the plug-in module. (This indication is visible when the front panel is closed.) The error pulse is also fed to the output of the receiver section where it can be used for an external alarm or for error counting.

For applications which do not require clock signals with the received data output, the 26C receive clock is not required. However, the receive clock is required for operation of the duobinary error detector.

EQUALIZING EQUIPMENT

Error rates in data transmission are minimized when delay and amplitude distortion introduced by the characteristics of the transmission line are reduced or eliminated. In addition to the adjustable delay equalizer which is an integral part of the 26C Data Set, an optional Delay Equalizer Shelf is available. This assembly incorporates a power supply, two line amplifiers, and six plug-in equalizer units. Normally, the Delay Equalizer is used when more than one transmission line must be equalized for use with the Data Set. For example, it can be adjusted to correct the delay and amplitude distortion for two voice circuits which have different transmission characteristics. Then the Data Set can be alternately connected or switched to either line without additional readjustment.

SYNCHRONOUS DUOBINARY FM

DUOBINARY CODING — Duobinary coding enables data to be transmitted at 2400 bits per second in the same bandwidth required for binary FM transmission at 1200 bits per second—in this case, over a voice channel with infinite attenuation at 600 and 3000 cps and 3 db attenuation at 1100 and 2500 cps.

The Duobinary technique is a signal design process that codes and shapes conventional binary data signals into a special waveform, characterized by three levels, as opposed to the two levels of a binary system.

The process of coding and shaping transforms binary MARKS and SPACES into the three discrete levels. Both the upper and lower levels represent MARKS, while the center level represents SPACES. The Duobinary signal differs from an ordinary three-level (or ternary) signal in that the particular level (upper or lower) occupied by each MARK does not occur randomly, but is determined, instead,

by a strict encoding pattern. As a consequence of predetermining the position of each MARK, the bandwidth required for transmission is reduced by one-half when compared to binary systems.

With the Duobinary principle, the marking frequency transmitted depends upon previous signals. If an odd number of spacing bits occur between marking bits, the new marking frequency will be opposite to that previously used. If an even number of spacing bits occur between marking bits, the new marking frequency will be the same as the marking frequency previously used.

Since the duobinary signal follows a definite pattern, violations of this pattern can be detected and interpreted by the Data Set receiver as errors caused by disturbances in the transmission path. Consequently, there is no need to add redundant digits to determine whether there are errors in encoding or in the line transmission facilities.

SYNCHRONOUS FM KEYING—In the 26C, data transitions are synchronized with those of the carrier wave. This greatly simplifies circuit design, thereby increasing reliability and reducing cost. In addition, since the input data digits are synchronized to the carrier frequency, intersymbol interference is negligible.

Carrier frequencies of 1200 and 2400 cps are used for 1200 bps binary FSK transmission. These carrier frequencies are derived from the 1200 cps transmit clock and no additional FM oscillator is required. (See figure 6.)

The 26C achieves 2400 bps duobinary transmission in a similar manner using the 2400 cps transmitter clock. (See figure 7.) In addition to simplifying circuit design, the synchronous FM keying technique also provides an important reduction in bandwidth because the data transitions occur at the same time as the carrier wave transitions. The signal energy is therefore grouped closely about the center frequency, and the bandwidth over which amplitude and delay distortion must be controlled is reduced.

In binary FM keying or non-synchronous keying, when a deviation ratio of one is used, approximately one-half the signal energy appears as discrete frequency components near the shifted frequencies. These discrete components do not contain useful information and the signal energy is wasted. However, in the 26C, synchronous duobinary FM keying is used and these discrete components do not occur. Therefore, information carrying components comprise the total signal and the effective signal energy is increased by 3 db. This in turn gives a performance improvement of 3 db in the error rate vs. signal-to-noise ratios.

When commonly used techniques, such as quaternary phase shift keying, are used to double the data rate within a given bandwidth, a penalty of 6 db in signal-to-noise ratio is incurred to achieve a given error rate. In the synchronous duobinary 26C, this penalty is less than 3 db. Figure 8 shows the error performance of the 26C at 1200 and 2400 bps data transmission rates.

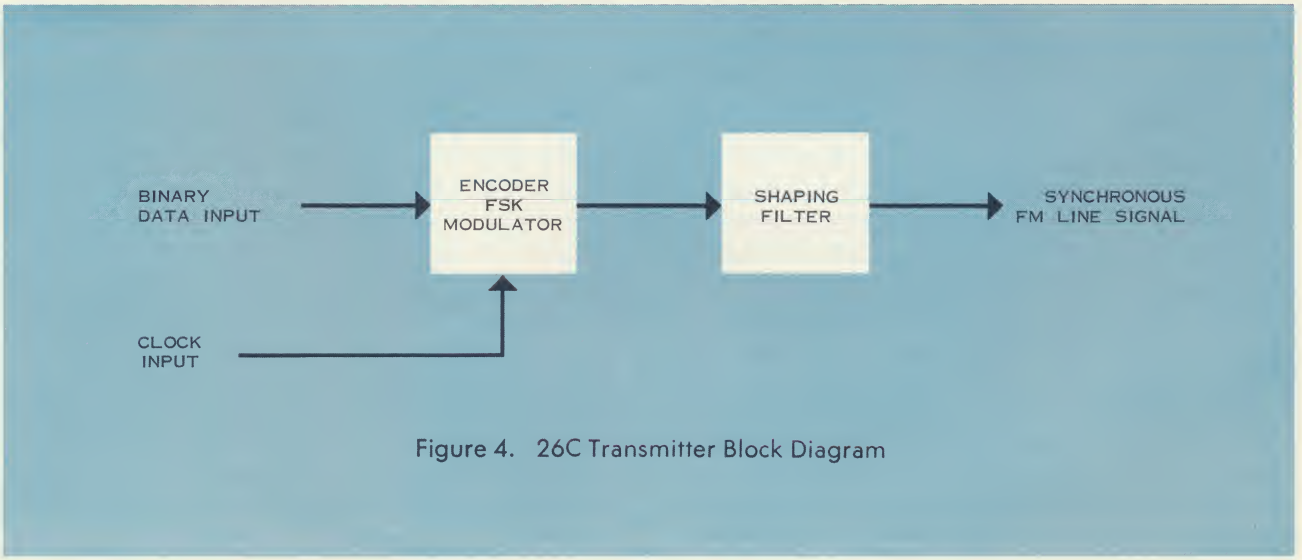

Figure 4. 26C Transmitter Block Diagram

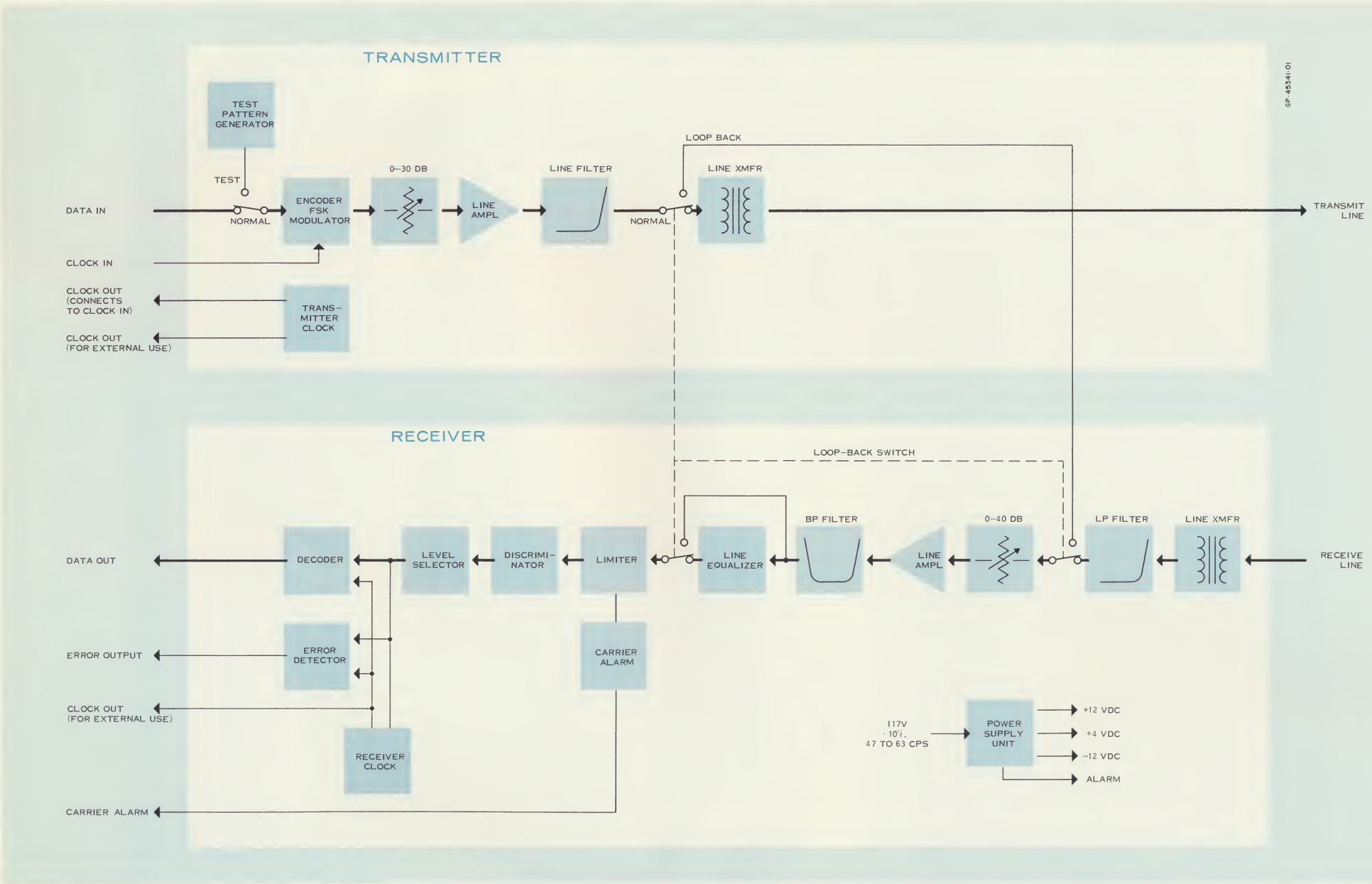

Figure 5. 26C Data Set Block Diagram

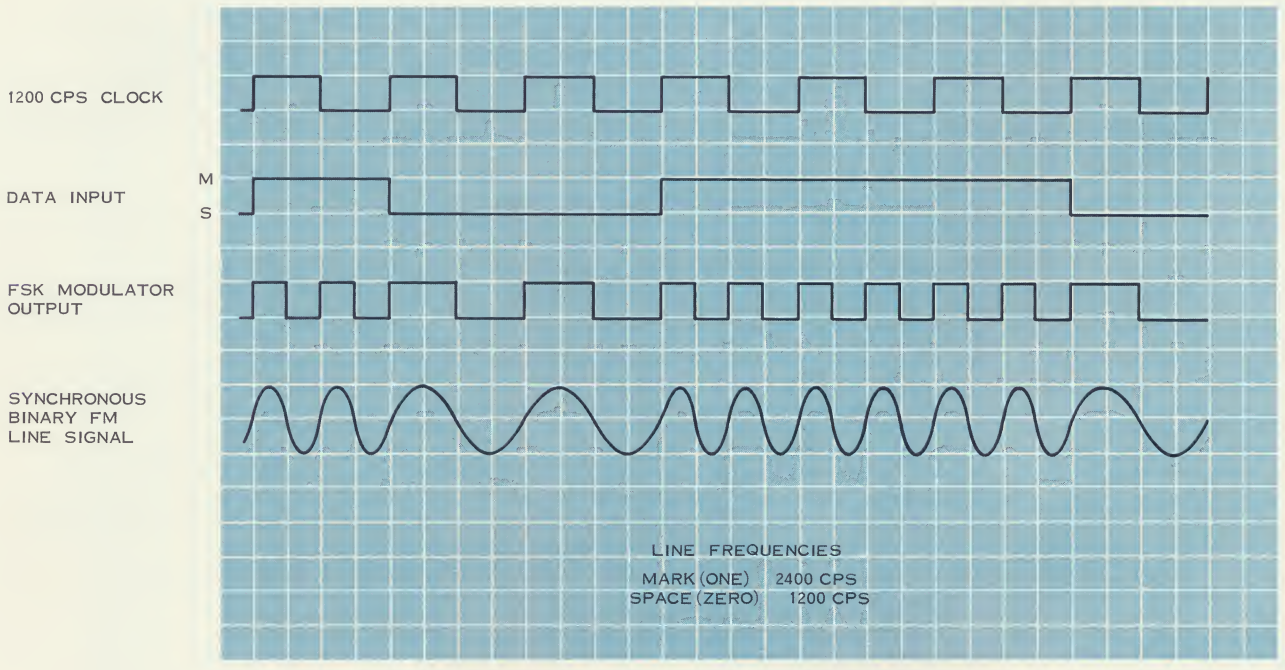

Figure 6. Synchronous Binary FSK Modulation Waveforms

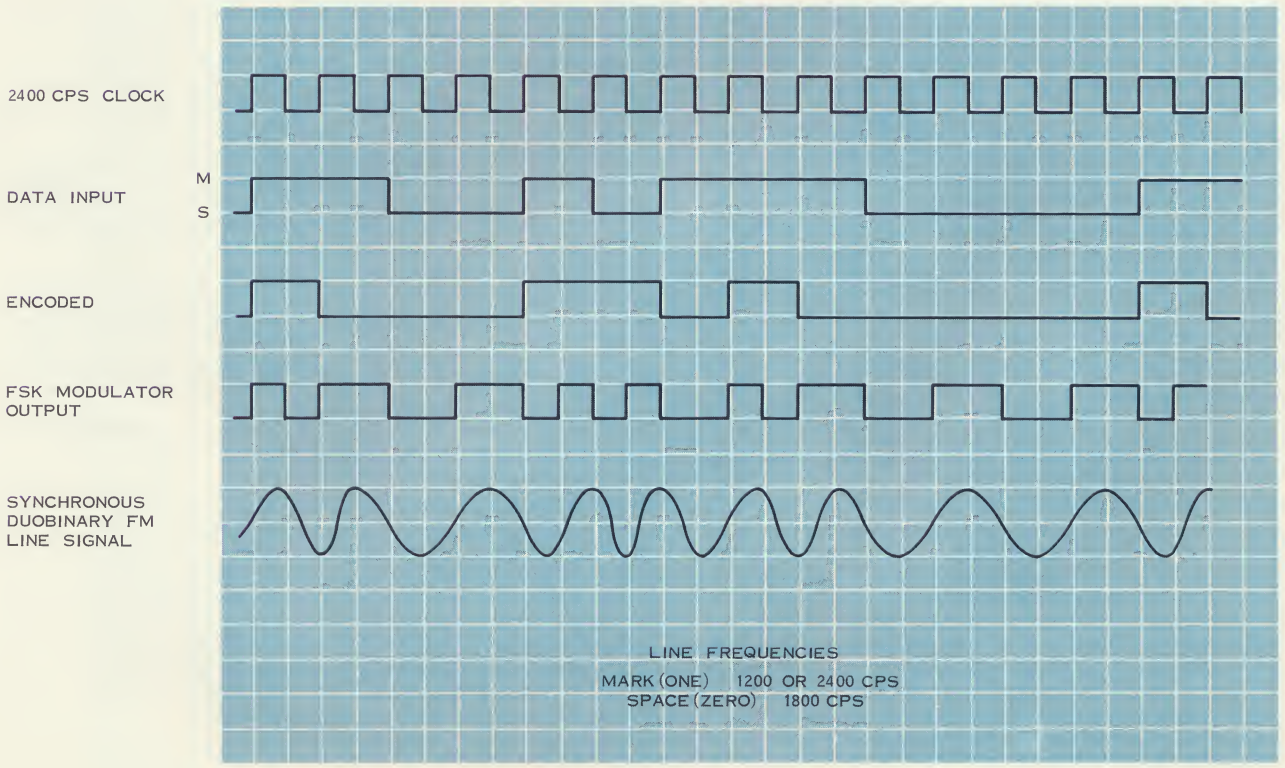

Figure 7. Synchronous Duobinary FSK Modulation Waveforms

TABLE A

Digital Data Input Strapping Options

Option	Mark (One)	Space (Zero)
1	−10v to −0.5v	+0.5v to +10v
2	−10v to −2.2v	−1.0v to +10v
3	−10v to +1.0v	+2.2v to +10v
4	+10v to +0.5v	−0.5v to −10v
5	+10v to −2.0v	−2.2v to −20v
6	+10v to +2.2v	+1.0v to −10v

NOTES:
1. For Input options 1 and 2, the positive and negative voltage operating points are within 10% of each other.
2. Strapping options are also provided to accept inputs of up to ±20v.

TABLE B

Digital Data Output Strapping Options

Option	Mark (One)	Space (Zero)
1	−6 ±1v	+6 ±1v
2	+6 ±1v	−6 ±1v

NOTES:
1. Mark and space output voltages are balanced to within 10% of each other.
2. With minor component changes other output voltage options can be provided to meet customer requirements. For example, 0 and +6v, 0 and −6v, or positive and negative values below or above ±6v can be provided.

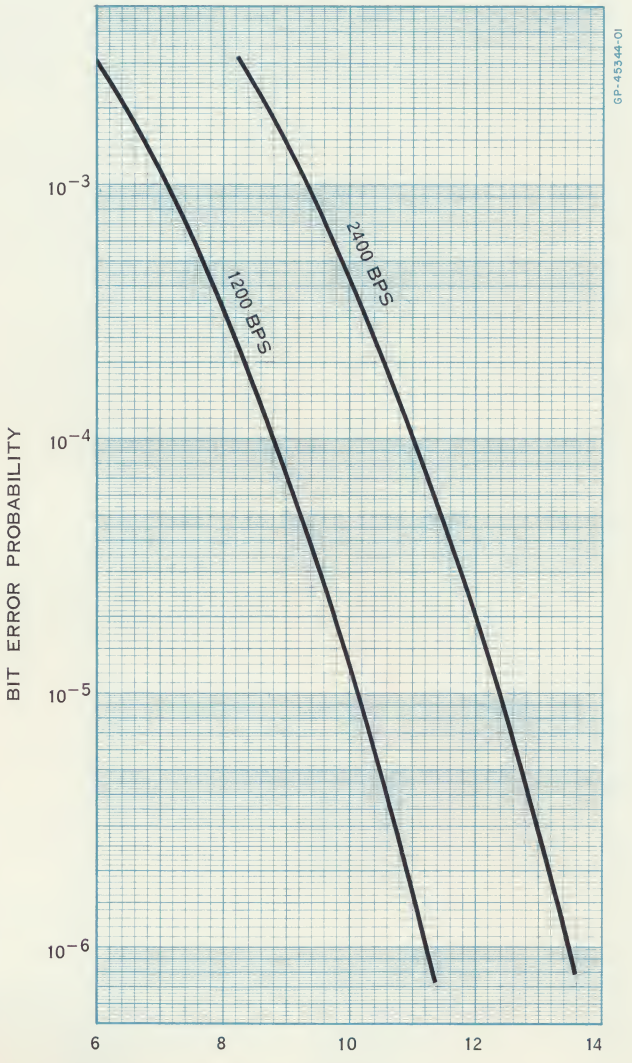

Figure 8. 26C Data Set Error Performance Curve

TABLE C

26C Data Set Equipment List

Type Number	Name	Type Number	Name
44750	Equipment Shelf	44757	Decoder, Error Detector Unit
44751	Power Supply Unit	44758	Receive Clock Unit
44752	Transmitter Unit	44763	Extender Unit
44753	Line Filter Receiver Unit	44764	Transmitter Clock Unit
44755	Adjustable Equalizer Unit	44765	Cabinet
44756	Limiter, Discriminator Unit		

NOTE: All units mount in the 44750 Equipment Shelf.

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TECHNICAL SUMMARY

DATA RATES	1200 or 2400 bits per second
DIGITAL DATA INPUT	
Input Line	Single wire, ground return
Format	NRZ serial binary data
Level Options	See Table A
Input Sensitivity	Voltage excursions (transients) up to 0.8v peak-to-peak do not affect operation of the Data Set
Input Impedance	Greater than 5000 ohms shunted by not more than 200$\mu\mu$f
Rise/Fall Times	Up to 200 μsec acceptable
DIGITAL DATA OUTPUT	
Output Line	Single wire, ground return
Format	NRZ serial binary data
Level Options	See Table B
Output Impedance	Less than 100 ohms at up to 10ma load current
Load Impedance	600 ohms minimum shunted by not more than 2500 $\mu\mu$f
Rise/Fall times	Between 1 and 2 μsec with provision for adding capacitor to increase rise time up to 10% of bit length
TRANSMIT (MODULATOR) LINE OUTPUT	
Signal	Synchronous FM
Frequency	1200 to 2400 cps nominal
Level	—10 to +6 dbm, adjustable
Impedance	300, 600, or 900 ohms balanced
RECEIVE (DEMODULATOR) LINE INPUT	
Signal	Synchronous or nonsynchronous FM
Frequency	1200 to 2400 cps nominal
Level	Adjustable to accept levels from 0 to —30 dbm (Short term variations up 10 db above and 20 db below the set level are acceptable)
Impedance	300, 600, or 900 ohms balanced
TRANSMITTER CLOCK OUTPUT	
Waveform	Square wave
Phasing	Positive or negative going edges coincide with data transitions (strapable)
Frequency	Same as bit rate
Level	±6v balanced to within 10%
Output impedance, load impedance and rise time	Same as data output
Frequency Stability	.01%
EXTERNAL TRANSMIT CLOCK INPUT (Required if Transmit Clock Module or Receiver Clock Shelf is not supplied)	
Waveform	Square wave, duty cycle 50% ±2%
Phasing	Negative edge at center of data bit
Frequency	Same as bit rate
Frequency Stability	0.01% minimum
Level	1v p-p to 40v p-p, ac coupled
Rise time	not more than 10% of bit length
RECEIVER CLOCK OUTPUT	
Waveform	Square wave
Phasing	Positive or negative going edges coincide with data transitions (strapable)
Frequency	Same as bit rate
Levels, output impedance, load impedance, and rise time	Same as data output
Frequency stability	Synchronized to transmitter clock
RECEIVER CLOCK SHELF OUTPUTS (May be used in place of the Transmit and Receive Clock Modules)	
Waveform	Square wave
Phasing	Positive or negative going edges coincide with data transitions (strapable)
Frequency	Same as bit rate
Level	±10 volts into 3000 ohm resistive load (other voltage options available)
Rise/fall times	1.0 μsec maximum
Frequency Stability	±5 parts in 10^8 for one hour
POWER SUPPLY ALARM (Optional)	Dry contacts activate alarm in event of any dc output failure
CARRIER ALARM OUTPUT	
Levels, output impedance and load impedance	Same as data output
TRANSMISSION LINE REQUIREMENTS	
Frequency Response Requirements	
(a) With built-in adjustable equalizer unit	—2 db to +6 db variation from 900 to 2700 cps
(b) Without adjustable equalizer unit	±1 db variation from 900 to 2500 cps
Enveloped Delay Requirements	
(a) With built-in adjustable equalizer unit	Within 1800 μseconds from 700 to 2700 cps
(b) Without adjustable equalizer unit	Within 300 μseconds from 900 to 2500 cps
Line Impedance	300, 600, or 900 ohms nominal at 1000 cps
Line S/N Ratio*	13 db at 2400 bps 10.5 db at 1200 bps
INTERFACE SYSTEM COMPATIBILITY	Conforms to EIA Standard RS-232-A data interface recommendations and meets the standard interface requirements (low level) of MIL-STD-188B.
TRANSMISSION FACILITIES	Operates over FCC Tariff 237 Schedule 4A telephone networks or any standard 3-kc voice channel derived on open-wire, cable, telephone carrier, or microwave radio transmission facilities.
POWER REQUIREMENTS	
Primary Power	117 vac ±10%, 47 to 63 cps
Power Consumption	15 watts maximum
ENVIRONMENTAL CONDITIONS (Operating)	
Ambient Temperature	0° to 50°C (32° to 122°F)
Relative Humidity	Up to 95%
Altitude	Up to 10,000 feet

*For a bit error rate of 1×10^{-5}
S = RMS Signal Power
N = RMS White (gaussian) noise power in a 3.4 kc band, flat weighting

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